CLAIMS:

What is claimed is:

1. A method of processing an interrupt disable instruction, comprising:

fetching an interrupt disable instruction including an operand specifying a number of cycles for disabling interrupt processing; and

executing the instruction.

2. The method according to claim 1 wherein the instruction operand is the number.

3. The method according to claim 1 wherein the instruction operand is a pointer to the number.

4. The method according to claim 1, wherein the pointer is stored in a register.

5. The method according to claim 1, wherein the operand identifies a register that stores the number.

6. The method according to claim 1, further comprising loading the number into a register.

7. The method according to claim 6, further comprising changing the number stored in the register based on processor cycles until the number reaches a predetermined value.

8. The method according to claim 7, wherein the changing is decrementing the number stored in the register.

9. The method according to claim 7, wherein the changing is incrementing the number stored in the register.

10. The method according to claim 7, wherein the predetermined value is zero.

11. The method according to claim 7, further comprising generating an interrupt disable signal during the changing of the number.

12. The method according to claim 11, further comprising generating an interrupt enable signal when the number reaches a predetermined value.

13. The method according to claim 7, further comprising writing the register with a value based on a write instruction.

14. A processor including an interrupt disable instruction processing feature, comprising:

a program memory for storing instructions including an interrupt disable instruction having an operand specifying a number corresponding to an interrupt disable duration;

a register for storing the number;

an instruction fetch/decode unit for fetching and decoding instructions, the instruction fetch/decode unit decoding the interrupt disable instruction and disabling the interrupt processing capability of the processor based on the number.

15. The processor according to claim 14, wherein the register changes the number based on processor cycles.

16. The processor according to claim 15, wherein the register changes the number by incrementing it.

17. The processor according to claim 15, wherein the register changes the number by decrementing it.

18. The processor according to claim 15, wherein the predetermined value is zero.

19. The processor according to claim 15, further comprising:

interrupt disable logic, coupled to the register, the interrupt disable logic generating an interrupt disable signal during the changing of the number.

20. The processor according to claim 15, wherein the interrupt disable logic generates an interrupt enable until the number reaches a predetermined value.

21. The processor according to claim 15, wherein a write instruction updates the register.